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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,550	06/27/2003	Edward A. Burton	INTEL-021	7414

34610 7590 06/12/2006

FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,550	BURTON ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-34,36,37,39,48-56 and 65-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-34, 36, 37, 39, 48-56, and 65-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the communications dated 03/16/2006 through 04/25/2006

Claims 31-34, 36, 37, 39, 48-56, and 65-67 are currently pending.

Claim(s) 1-30, 35, 38, 40-47, and 57-64 have been cancelled.

Remarks

2. Applicant's arguments filed on 03/16/2006 have been fully considered, but are moot in view of the new ground of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim(s) 31-34, 36, 37, 39, 48-56, and 65-67 is/are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,885,043 to Smith et al.

Regarding claim 31, Smith discloses a semiconductor device, comprising:

a first set of signal wires (see figs. 6-8, and the attached figure below), including a first plurality of signal wires 604 distributed in a first layer and a second plurality of signal wires 606 distributed in a second adjacent layer;

a second set of signal wires, including a third plurality of signals wires 604 distributed in the first layer and a fourth plurality of signal wires (606) distributed in the second layer, the first and second sets having a different number of signal wires, with the signal wires in the first set being substantially parallel and arranged in a first pattern, and the signal wires in the second set being substantially parallel and arranged in a second pattern.

Regarding claim 32, Smith discloses the semiconductor device wherein each of the first and second sets have an even number of signal lines. See fig. 6.

Regarding claim 33, Smith discloses the semiconductor device wherein the first layer has a number of signal wires from the first and second sets different from a number of signal wires from the first and second sets in the second layer (fig. 6 shows that the first layer has signal segments 604a/604b).

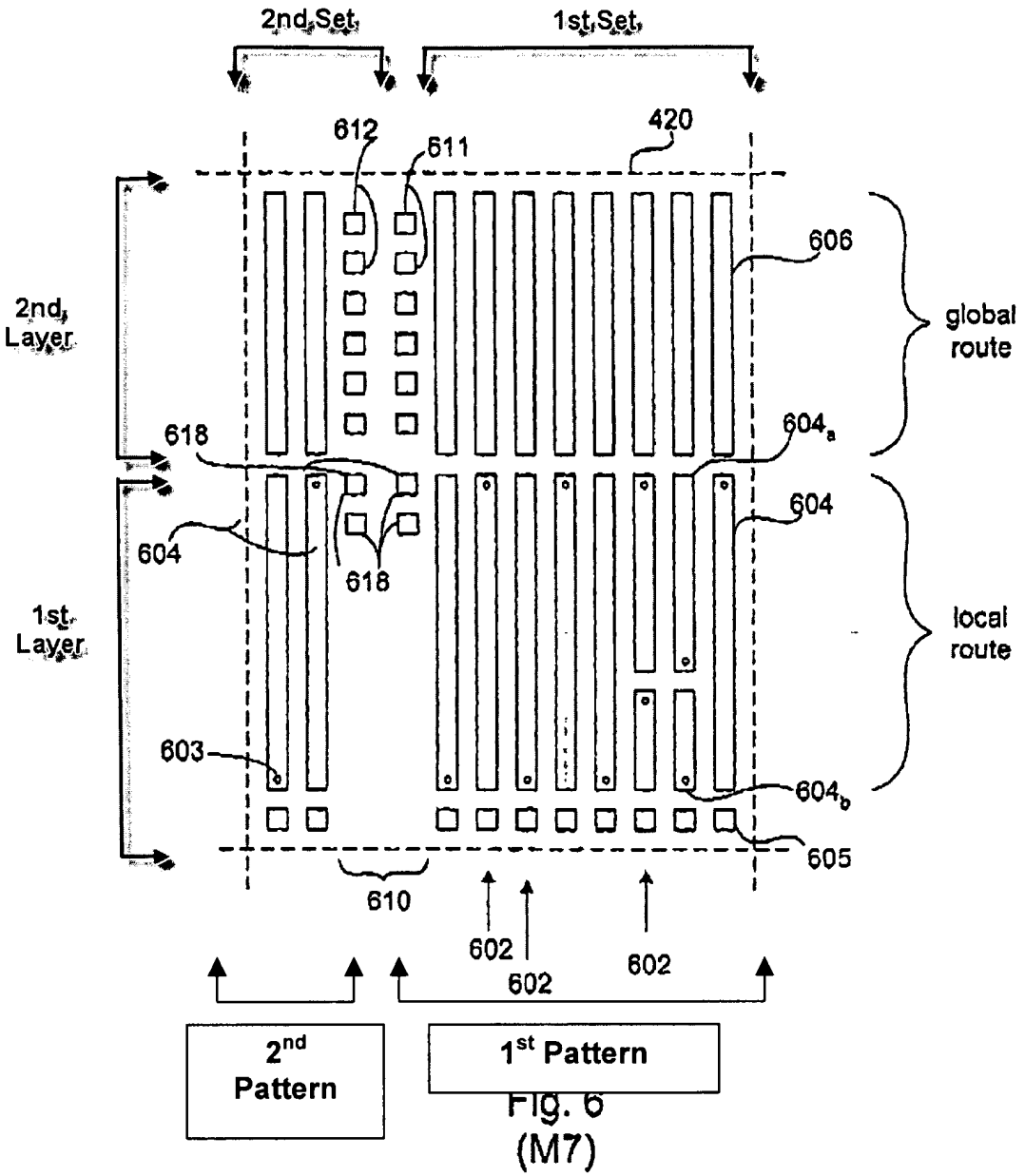


Fig. 6
(M7)

Regarding claim 34, Smith discloses the semiconductor device wherein the first and second patterns are a same pattern (both are in the same pattern 420, fig. 6).

Regarding claim 36, Smith discloses the semiconductor device wherein the first and second patterns are alternating patterns (1st Pattern and 2nd Pattern as shown in the above figure).

Regarding claim 37, Smith discloses the semiconductor device wherein the number of signal wires in the first layer of the first set is different from the number of signal wires in the first layer of the second set. See figs. 6-8.

Regarding claim 39, Smith discloses the semiconductor device wherein the first and second layers are adjoining layers. See figs. 6-8.

Regarding claim 48, Smith disclose the semiconductor device wherein signal wires in the first layer are local interconnect wires and signal wires in the second layer are global routing wires. See fig. 6.

Regarding claim 49, Smith discloses the semiconductor device wherein the signal wires in the first set have a same permittivity and the signal wires in the second set have a same permittivity. This is inherent because they are of the same material.

Regarding claim 50, Smith discloses the semiconductor device wherein the first set of signal wires is separated from thee second set of signal wires. See fig. 6.

Regarding claim 51, Smith discloses the semiconductor device wherein the first set of signal wires is separated from the second set of signal wires by one or more ground or return wires. See fig. 10.

Regarding claim 52, Smith discloses the semiconductor device wherein the first set of signal wires is separated from the second set of signal wires by ground or return wires in the first and second layers. See fig. 10.

Regarding claims 53-56, Smith discloses the semiconductor device comprising all claimed limitations. See fig. 10.

Regarding claim 65, Smith discloses the semiconductor device wherein the first layer is formed over the second layer. See figs. 1, 6-10.

Regarding claim 66, Smith discloses the semiconductor device wherein the signal lines in the first and second sets are oriented in a same direction. See figs. 6-10.

Regarding claim 67, Smith discloses the semiconductor device wherein the signal lines in the first and second sets ate parallel to one another. See figs. 6-10.

5. Claim(s) 31, 53, 54, and 65-67 under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,329,604 to Koya.

Regarding claim 31, Koya discloses a semiconductor device, as shown in figs. 2, 3 and 6-10, comprising:

a first set of signal wires (on the left of the dash line shown in the attached figures below), including a first plurality of signal wires 74 distributed in a first layer 45 or 74 (alternately, 1' layer 42 or 73) and a second plurality of signal wires 84 distributed in a second adjacent layer 42 or 73 (alternately, 2' layer 41 or 71);

a second set of signal wires (on the right of the dash line), including a third plurality of signals wires 74 distributed in the first layer and a fourth plurality of signal wires 84 distributed in the second layer 73, the first and second sets having a different number of signal wires, with the signal wires 73, 74 in the first set being substantially parallel and arranged in a first pattern, and the signal wires 73, 74 in the second set being substantially parallel and arranged in a second pattern.

Regarding claim 53, Koya discloses the device wherein the first set of signal wires 74 is located between the one or more ground or return wires 72 and one or more power supply wires 75. See figs. 9-16.

Regarding claim 54, Koya discloses the device wherein the second set of signal wires 73 is located between the one or more ground or return wires 72 and one or more additional power supply wires. See figs. 9-16.

FIG. 9

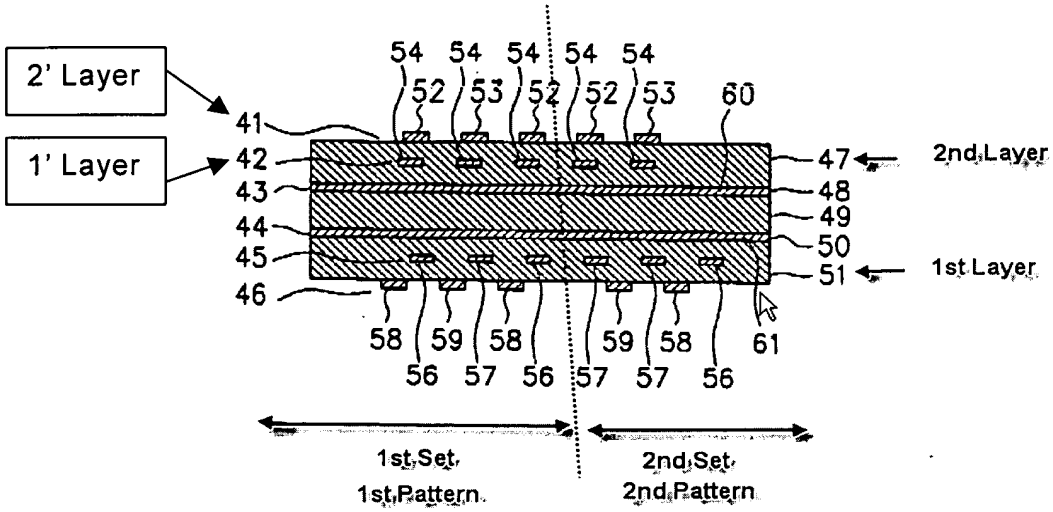
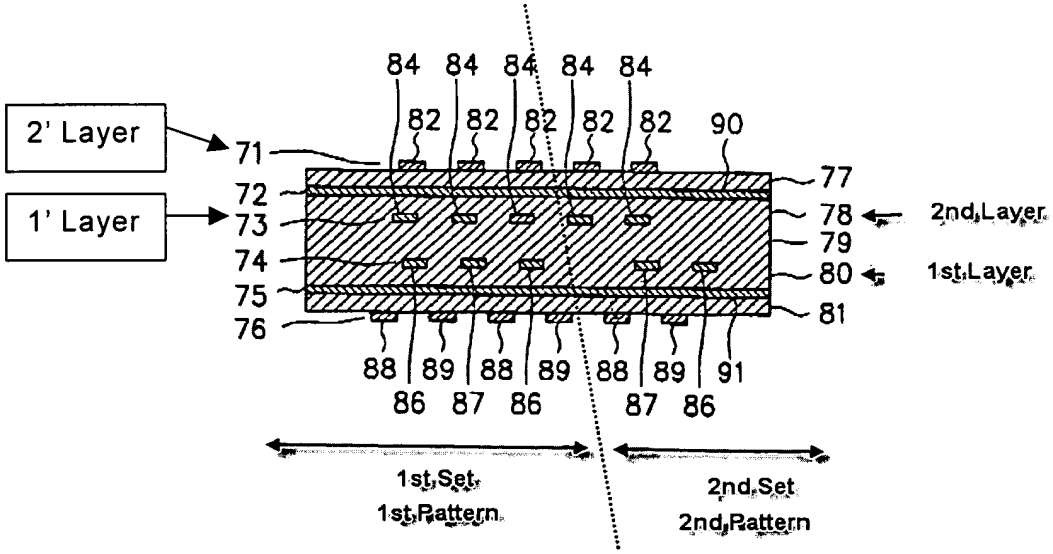

2' Layer
1' Layer
41
42
43
44
45
46
47
48
49
50
51
54 54 54 54 54
52 53 52 52 53
60
58 59 58 59 58
56 57 56 57 57 56
61
2nd Layer
1st Layer
1st Set
1st Pattern
2nd Set
2nd Pattern

FIG. 10


2' Layer
1' Layer
71
72
73
74
75
76
77
78
79
80
81
84 84 84 84 84
82 82 82 82 82
90
88 89 88 89 88 89 91
86 87 86 87 86
2nd Layer
1st Layer
1st Set
1st Pattern
2nd Set
2nd Pattern

Regarding claim 65, Koya discloses the semiconductor device wherein the first layer is formed over the second layer. See figs. 9, 10.

Regarding claim 66, Koya discloses the semiconductor device wherein the signal lines in the first and second sets are oriented in a same direction. See figs. 9,10.

Regarding claim 67, Smith discloses the semiconductor device wherein the signal lines in the first and second sets ate parallel to one another. See figs. 9, 10.

Conclusion

6. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571)272-1907. The fax numbers for all communication(s) is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

ANDY HUYNH
PRIMARY EXAMINER

Dao H. Nguyen
Art Unit 2818
June 5, 2006